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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/614,031      | 07/08/2003  | James N. Pan         | 50432-592           | 6675             |

7590 01/19/2005  
McDERMOTT, WILL & EMERY  
600 13th Street, N.W.  
Washington, DC 20005-3096

| EXAMINER |
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STEVENSON, ANDRE C

| ART UNIT | PAPER NUMBER |
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2812

DATE MAILED: 01/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/614,031

Applicant(s)

PAN ET AL.

Examiner

Andre' C. Stevenson

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 October 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 12-18 is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☒ Claim(s) 4-11 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

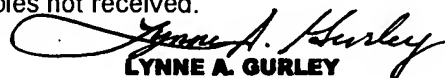
**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

  
LYNNE A. GURLEY

PRIMARY PATENT EXAMINER  
TC 2800, AU 2812

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### Response to Applicant's Arguments

Applicant's arguments, see pages 5 through 8, filed 10/26/04, with respect to the rejection(s) of claim(s) 1 through 18 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Rao et al. and Yonehara et al..

#### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over G. Venkata Rao et al ("Characteristics of Al/p-Cu<sub>0.5</sub>Ag<sub>0.5</sub>InSe<sub>2</sub> Polycrystalline Thin Film Schottky Barrier Diodes") in view of Yonehara et al (U.S. Pat 5,219,769 B2)

Rao shows the method substantially as claimed in pages 571 through. 576:

Pertaining to claim #1, Rao shows a method of determining a work function of a metal (Fig. #3, page 575, Section 4 "conclusion"), comprising the steps of: forming a Schottky diode (metal-on-glass) with a metal having a work function to be determined forming contacts of the MS Schottky diode', measuring a capacitance-voltage curve of the MS Schottky diode; and

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determining the work function of the metal based on the measured capacitance-voltage curve, (Fig. #3, page 572, paragraph 2).

Rao fails to show, with respect to claim 1, forming a metal-on-silicon (MS) Schottky diode.

Yonehara teaches with respect to claim 1, forming a metal-on-silicon (MS) Schottky diode. Although diamond substrates are exemplified, Yonehara teaches conventional substrates which are used to form a Schottky diode, which include silicon or glass substrates as equivalents or alternates (column 5, lines 49 through 59, column 4, lines 45 through 50).

It would have been obvious to one having ordinary skill in the art, at the time the invention was made, to substitute a silicon substrate for the glass substrate, in the method of Rao, to form a metal-on-silicon (MS) Schottky diode, with the motivation that Yonehara explicitly teaches silicon substrate as a conventional equivalent or alternate to a glass substrate. Therefore, the silicon substrate should provide similar results to the glass substrate regarding device performance.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over G. Venkata Rao et al ("Characteristics of Al/p-Cu<sub>0.5</sub>Ag<sub>0.5</sub>InSe<sub>2</sub> Polycrystalline Thin Film Schottky Barrier Diodes") in view of Yonehara et al (U.S. Pat 5,219,769 B2), as applied to claim 1 above, and further in view of Bastasz et al (U.S. Pat 4,782,302).

Rao in view of Yonehara shows the method substantially as claimed and as stated in the previous paragraphs.

Rao in view of Yonehara fails to show, with respect to claim 2, the method of claim 1, wherein the step of forming the MS Schottky diode includes depositing the metal on a silicon substrate in accordance with a mask on the silicon substrate, and with respect to claim 3, the method of claim 2, wherein the mask is a shadow mask.

Bastasz teaches with respect to claim 2, the method of claim 1, wherein the step of forming an MS Schottky diode includes depositing a metal on a silicon substrate in accordance with a mask on the silicon substrate, and with respect to claim 3, the method of claim 2, wherein the mask is a shadow mask (column 2, lines 25 through 47). Specifically Bastasz teaches a conventional process of depositing a metal, using a shadow mask to form an (MS) Schottky diode on a silicon substrate.

It would have been obvious to one having ordinary skill in the art, at the time the invention was made, to have had the step of forming the MS Schottky diode include depositing the metal on a silicon substrate in accordance with a mask on the silicon substrate, and to have had the mask be a shadow mask, in the method of Rao in view of Yonehara, with the motivation given by Bastasz, since Bastasz states, in column 2, lines 30 through 57, that conventionally a series of masks are placed over a diode array in succession to enable a build up of metal layers on selected diodes with exclusion of metal film build up on other diodes or areas during metal deposition to form a (MS) Schottky diode.

### **Allowable Subject Matter**

Claims 4 through 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims subject to an updated search.

Claim #4 allowable subject matter:

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- ✓ Contact is at least ten times smaller in size than a second one of the contacts.

Claim #9 allowable subject matter:

- ✓ Contacts are actual capacitor contacts and another one of the contacts is a front contact.

Claims 12 through 18 are allowed.

The following is an examiner's statement of reasons for allowance: While the prior art teaches positioning a shadow mask having holes on a silicon substrate, depositing the metal through holes in the shadow mask, it fails to teach "a second hole with a second cross-sectional area that is at least 100 times greater than the first cross-sectional area" (claim 12).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866 - 217 - 9197 (toll-free).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre C. Stevenson whose telephone number is (571) 272 1683. The examiner can normally be reached on Monday through Friday from 8:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 7724.


Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 1782. Also, the proceeding numbers can be used to fax information through the Right Fax system;

- **703 872 9306**

Andre C. Stevenson

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1/14/05

  
**LYNNE A. GURLEY**  
**PRIMARY PATENT EXAMINER**  
**TC 2800, AU 2812**